

**本科实验报告**

|  |  |
| --- | --- |
| 课程名称： | 计算机组成 |
| 姓 名： | TANG ANNA YONGQI |
| 学 院： | 计算机科学与技术学院 |
| 专 业： | 计算机科学与技术（中加班）留学生 |
| 学 号： | 3180300155 |
| 生活照： |  |
| 指导教师： | 刘海风，洪奇军 |

2020年 4月10日

Lab 5 – Datapath Design

**Name:** Anna Yongqi Tang **ID:** 3180300155 **Major:** 计算机科学与技术（中加班）留学生

**Course:** Computer Organization

**Date:** 2020-04-10 **Instructor:** 洪奇军

1. **Method and Experimental Steps**

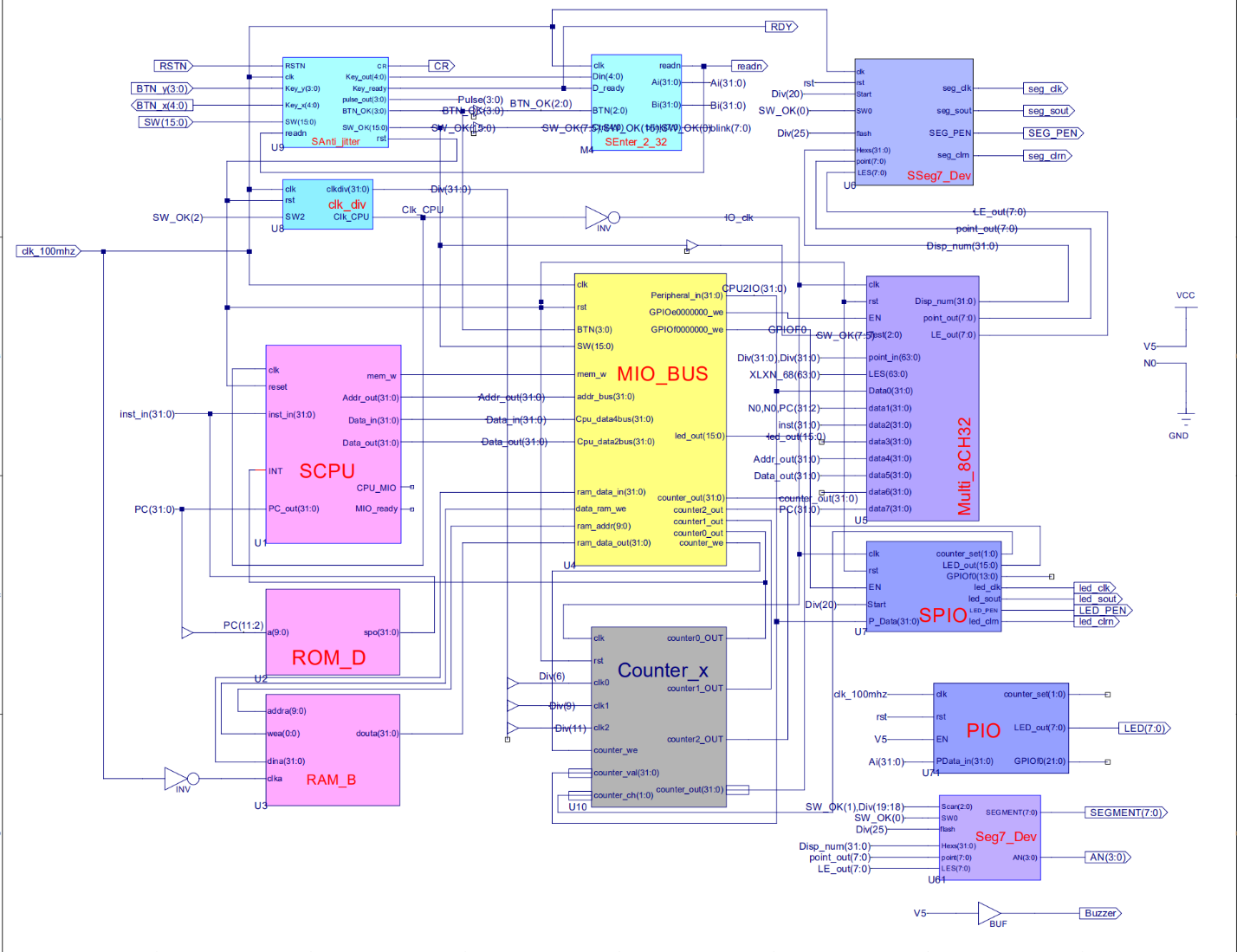


Figure 1 - topMod.sch

This depicts the completion of lab 5. The purpose of this week’s experiment was to explore the different components of a datapath, and better understand how a processor works in a single cycle implementation. In this lab, I took lab 4 and I modified the datapath unit of the SCPU. In the datapath that we have constructed this week, it consists of a PC, adders to calculate target addresses, MUXes to handle different signals, a sign extender, a register file and an ALU which were from the last lab. There are five MUXes and seven different control signals to handle instruction processing. Instruction memory and data memory were not implemented in this week’s lab. The .ucf for this program came from the provided courseware, and is linked to topMod.sch. Synthesis had minimal warnings, and implementation was successful. A programmable file has been generated and is ready for testing on the SWORD board.

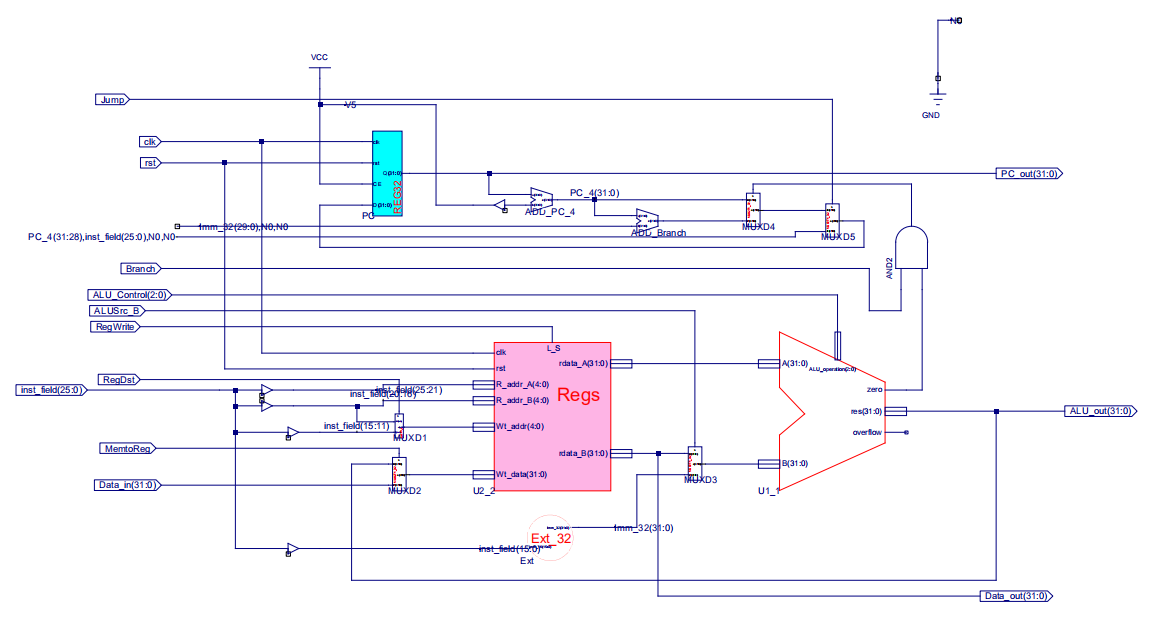


Figure 2 – Data\_path.sch

The above picture is a schematic of the datapath module of the SCPU. As we can see, there are several control signals and MUXes used. In this implement, the memory read and write signals are omitted. The datapath operates differently depending on the type of instruction fetched. The control signals have different assertions depending on instruction class. These signals determine which components are used, and how data flows in the path.



Figure 3 – 3180300155\_TANGANNAYONGQI\_05

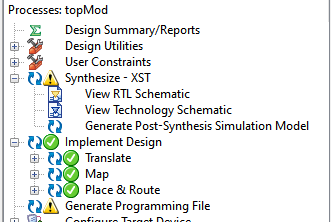
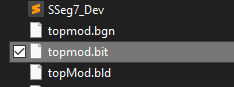
 

Figure 4 - .bit file generation Figure 5 - .bit file generated in directory

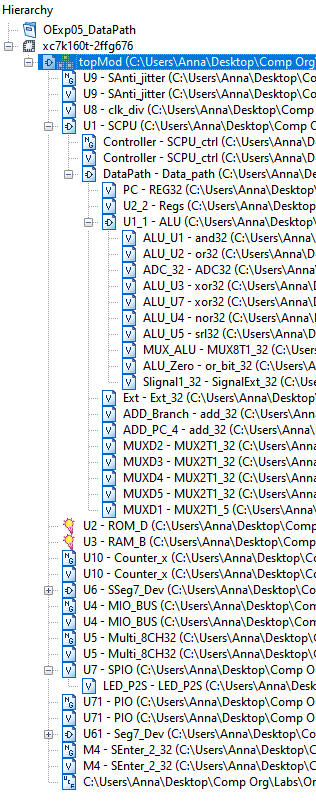


Figure 6 - file hierarchy

**2. Simulations and Observations**

This lab requires a MIPS program to be designed and tested on the datapath. The DEMO program and datapath testing will be performed later. The error observed in the ALU from last lab has been fixed, and I have re-simulated it using the Verilog test fixture that I have previously produced. I have also simulated the datapath by adjusting the control signals for each instruction that it currently supports.

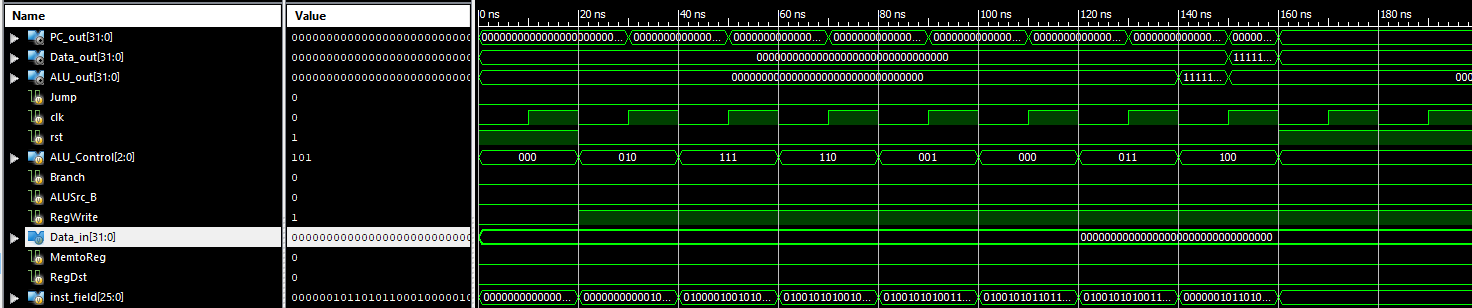


Figure 7 – Datapath Simulation

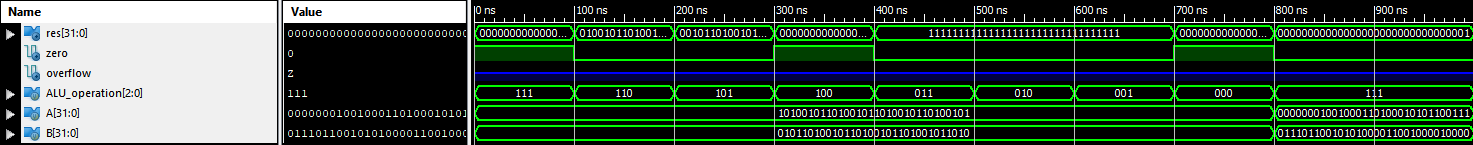


Figure 8 – Revised ALU Simulation

*Datapath Simulation*

module Data\_path\_Data\_path\_sch\_tb();

// Inputs

reg Jump;

reg clk;

reg rst;

reg [2:0] ALU\_Control;

reg Branch;

reg ALUSrc\_B;

reg RegWrite;

reg [31:0] Data\_in;

reg MemtoReg;

reg RegDst;

reg [25:0] inst\_field;

// Output

wire [31:0] PC\_out;

wire [31:0] Data\_out;

wire [31:0] ALU\_out;

// Bidirs

// Instantiate the UUT

Data\_path UUT (

.PC\_out(PC\_out),

.Jump(Jump),

.clk(clk),

.rst(rst),

.ALU\_Control(ALU\_Control),

.Branch(Branch),

.Data\_out(Data\_out),

.ALUSrc\_B(ALUSrc\_B),

.RegWrite(RegWrite),

.ALU\_out(ALU\_out),

.Data\_in(Data\_in),

.MemtoReg(MemtoReg),

.RegDst(RegDst),

.inst\_field(inst\_field)

);

// Initialize Inputs

initial begin

`define signals {RegDst,ALUSrc\_B,MemtoReg,Jump,Branch,RegWrite,ALU\_Control}

Branch = 0;

clk = 0;

rst = 1;

ALU\_Control = 0;

ALUSrc\_B = 0;

RegWrite = 0;

Jump = 0;

MemtoReg = 0;

inst\_field = 0;

Data\_in = 0;

RegDst = 0;

#20;

rst=0;

//add

`signals=12'b100000001010;

inst\_field=26'b00000000000100000000100000;

#20;

//slt

`signals=12'b100000001111;

inst\_field=26'b01000010010101000000101010;

#20;

//sub

`signals=12'b100000001110;

inst\_field=26'b01001010100101100000100010;

#20;

//or

`signals=12'b100000001001;

inst\_field=26'b01001010100110000000100101;

#20;

//and

`signals=12'b100000001000;

inst\_field=26'b01001010110110100000100100;

#20;

//xor

`signals=12'b100000001011;

inst\_field=26'b01001010100111000000100110;

#20;

//nor

`signals=12'b100000001100;

inst\_field=26'b00000010110100100000100111;

#20;

//srl

`signals=12'b111000001101;

inst\_field=26'b00000010110101100010000010;

rst=1;

end

always begin

clk=0;#10;

clk=1;#10;

end

endmodule

**3. Conclusion**

In this week’s lab and theoretical section of this course, we got to explore and build a datapath from scratch and look at how different instruction types process data from the register file in a single cycle. I also got to look at how read and write in memory and the register file worked. We haven’t gotten the chance to implement memory into this datapath yet, but I’m looking forward to that. I’m also looking forward to implementing this onto actual hardware, and physically witnessing how computer processes work. Last summer, I took Yale Patt’s Computing System’s course and I’m glad that I got to revisit this concept again. It was cool to see the differences in the course of action of the LC-3 and the kintex7. I’m looking forward to experimenting with the further continuations of this lab.

1. **Source Code**

All modules and components were either retrieved from previous labs or directly taken from the given files.